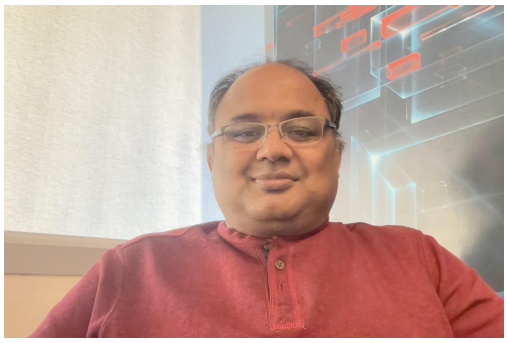
2024 P4 Technical Steering Team (TST) Nominees

Fernando Ramos

- **LinkedIn or Bio:**
  - I am an Associate Professor at Instituto Superior Técnico, University of Lisbon (ULisboa), where I teach computer networking (mainly), systems, and computer architecture topics. I am the coordinator of our Master's Programme on Telecommunications and Informatics Engineering. I am a senior researcher at INESC-ID, where I head the Distributed, Parallel, and Secure Systems Scientific Area, a research group of 130+ people, including ~20 faculty members. Previous positions include teaching and research roles at the Faculty of Sciences ULisboa, University of Cambridge, Telefonica Research, and Altice Labs. I hold a PhD from the University of Cambridge and an MSc from the Queen Mary University of London. I have participated in 10+ international projects and am currently the coordinator of the ACES project (an 8M€ EU Horizon project) and PI of the FCT-funded project Myriarch. I am the co-author of 60+ scientific publications, totaling 7900+ citations (GSC) at this date.
- **How long have you been working on the P4 Project?**
  - My involvement with the P4 project started in 2018, with initial contributions to the P4 Education WG.
- **What contributions have you made in the past to the P4 Project?**
  - My main contributions are related to using P4 in Education and promoting P4 in Europe. Specifically:
    - I am chair of the P4 Education WG (since 2021)
    - I was involved in the organization of the six EuroP4 workshops in Europe (five as PC co-chair or organization co-chair)
    - I was involved in the organization of the P4Pi hackathon in SIGCOMM'22 and the P4 tutorial in NetSoft'22
- **What are you actively working on in the P4 project?**
  - I am currently the P4 Education WG Chair and am co-organizer of the EuroP4'23 workshop (with CoNEXT'23 in Paris).

- **Why do you feel you would be a good candidate for this position?**
    - I have 20+ years of experience teaching and researching computer networking. I introduced P4 in my advanced computer networking course back in 2015, and since then I have done research involving P4 on various topics, including monitoring (FlowLens, NDSS'21), security (Peregrine, poster@SIGCOMM'23), and network function synthesis (SyNAPSE, SOSR'22; Maestro, NSDI'24). My leadership, organizational, and coordination skills may also be helpful for this position.
- **Are there any changes you would like to bring to the community if elected into this position?**
    - I would not call these changes, but I would emphasize two areas in particular if elected:
        - Promote the use of P4 for computer networking education, for instance by helping aggregate and curate existing material and also by creating new material for different types of courses. This is an important goal we already set in the context of the P4 Education WG.
        - Continue promoting the evolution of P4 from a "switch-centric" language towards a more general language for packet processors, including NICs (P4 Portable NIC Architecture) and host packet processing (e.g., P4TC).

Hari Thantry

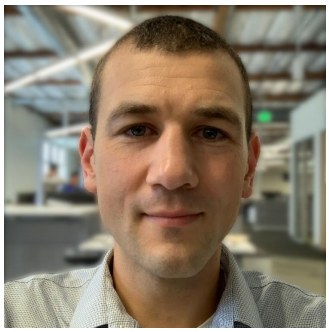


- **LinkedIn or Bio:**
    - https://www.linkedin.com/in/hariharan-thantry-01b731/
- **How long have you been working on the P4 Project?**
    - Have been working on the P4 project since 2015, 2015-16 at Barefoot (BMv2, backend parser), 2016-19 at Fungible, building a backend for their chip (no open source), and since 2020 @ Google, contributing mostly to furthering the P4-PNA agenda, and proposing language changes to enable SmartNIC use cases (for loops, connection tracking, LUT tables in actions).
- **What contributions have you made in the past to the P4 Project, and what are you actively working on?**
    - Currently, I'm leading the effort @Google on using P4 as the standardized language for expressing all our fastpath pipelines, and as the preferred

infrastructure for a vendor-agnostic HAL. I'm also engaged externally in improving the open source support for targeting real hardware, for e.g. through adding compiler passes to the existing P4C frontend to enable targeting a TCAM based parser model, based on http://yuba.stanford.edu/~nickm/papers/ancs48-gibb.pdf. Artifacts: The parser model is published: https://github.com/google/cairn, and the compiler changes are being worked on (in collaboration with Anirudh Sivaraman). Some earlier work in this space was done a few years ago (by us), but was not merged in because we wanted to fix the idea of being able to describe hardware constraints for TCAM architectures: https://github.com/p4lang/p4c/pull/2898

- **Why do you feel you would be a good candidate for this position?**
    - Having worked fairly deeply in both Switch (Tofino @Barefoot), and programmable SmartNICs (F/S1 @Fungible, Mount evans @Google), and having worked fairly closely with vendors on other architectures (Pensando Elba & Nvidia Bluefield), I feel that I bring a fairly unique perspective to both the set of challenges & the opportunities in evolving P4 for emerging SmartNIC architectures. I believe that for P4 to be successful in the SmartNIC space, it should evolve in a direction that allows expressing endpoint operations (e.g. descriptor processing, TSO, DMA) and primitives (timers, queues) at a fairly fine grained level. Steering P4 to work with emerging silicon in this space, while also strengthening the open source ecosystem around it (compilers, models) would greatly accelerate the adoption of such silicon.
- **Are there any changes you would like to bring to the community if elected into this position?**
    - As a community, I believe it's imperative for us to focus on evolving the language, the compiler, and the models to meet new emerging use cases that can be targeted on domain specific silicon. Strengthening the open source ecosystem would drive the key to greater adoption of P4 in these newer areas (SmartNIC).

Nate Foster



- **LinkedIn or Bio:**
    - https://www.cs.cornell.edu/~jnfoster/bio/
    - https://www.linkedin.com/in/nate-foster-935795125/

- **How long have you been working on the P4 Project?**
    - I first got involved with P4 in 2016.
- **What contributions have you made in the past to the P4 Project?**
    - I currently serve as co-chair of the Language Design Working Group. On the technical side, I've been involved with tools for reasoning about P4 programs, including p4v, Petr4, LeapFrog, and p4testgen. The latter tool, led by Fabian Ruffy, has seen significant adoption in industry.
- **What are you actively working on in the P4 project?**
    - With my Cornell research group, I've been working on a formal specification of the language. In the open-source community, I'm excited about the emerging effort led by Andy Fingerhut to bring architecture specifications into the language.
- **Why do you feel you would be a good candidate for this position?**
    - I'm eager to help P4 continue to develop to achieve maximum impact in the industry. In my view, this means consolidating efforts around P4 on switches, evolving the language to support P4 on NICs, and continuing to support work on P4 as a specification language.
- **Are there any changes you would like to bring to the community if elected into this position?**
    - I believe it's important to clearly articulate a technical roadmap, both for design and open-source software, and to grow the set of active contributors. One way to achieve this could be to focus the community's efforts through a smaller set of integrated meetings.

Steffen Smolka

- **LinkedIn or bio:**
    - https://www.linkedin.com/in/steffen-smolka/
- **How long have you been working on the P4 Project?**
    - I first started working on P4 in 2016 as an intern at Barefoot networks. For the last 4 years, since Jan 2020, I have been working on P4 at Google.
- **What contributions have you made in the past to the P4 Project?**

    - See https://opennetworking.org/news-and-events/blog/2021-p4-tst-election-results/.
- **What are you actively working on in the P4 Project?**
    - At Google, I lead a team that uses P4 as a specification language and builds & and applies tools that perform automated switch validation against such a given P4 spec. We have published a paper describing this approach at SIGCOMM last year, and have given a tutorial (together with many external collaborators) on it at SIGCOMM this year.
- **Why do you feel you would be a good candidate for this position?**
    - I am actively using P4 on a daily basis. Working at Google, I represent an important industrial player in the space. I can offer both an industrial/practical perspective (as a Google SWE) and well as an academic/theoretical perspective (having done a PhD in programming languages).
- **Are there any changes you would like to bring to the community if elected into this position?**
    - I'd like to build more awareness around & momentum behind the usage of P4 as a specification language. In my view, this use case is still under-emphasized. With Tofino out of the picture, it may become the most appealing P4 use case going forward.